Plasma-Induced Oxide Damage:
A Status Report

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I. BACKGROUND

In the last five years, the rapid development of microelectronics is apparent to all because of the prevalence of fast personal computers, cellular phones, electronic banking, automotive controls, and small electronic gadgets. The advances in miniaturization of integrated circuits has been made possible by the use of plasmas (ionized gases) in the etching of fine features in semiconductor chips and the deposition of insulating and conducting layers into small spaces. Complicated computer chips such as the Pentium Pro, containing more than 5 million transistors, are made hundreds at a time on a round "wafer" of silicon, presently 8 inches (200 mm) in diameter. For reasons of economy and computing speed, the "die size", or area of each chip, has to be kept to 50-60 mm^2. Future chips, therefore, have to have even smaller feature size and incorporate many interconnected layers; and, since hundreds of processing steps are involved, larger wafers have to be used so that more can be made at a time. The Semiconductor Industry Association's National Technology Roadmap calls for decreasing the feature size from 0.35 to 0.25 μm by 1997, to 0.18 μm by 2001, and to 0.10 μm by 2007. The 0.25 μm goal was achieved ahead of schedule, and 0.18 μm etching has been demonstrated in the laboratory. However, to advance beyond this, a deeper understanding of plasma processing has to be attained.

Up to now the problem has been to generate high density plasmas (HDPs) that can cover large areas so that wafer sizes can be increased to 300-400 mm. A second problem is to avoid the generation of particulates ("dust"), which can fall onto a chip and decrease the yield. Several HDP tools have been developed, and these not only provide dense, uniform plasmas but also eliminate the dust by operating at low neutral pressures. One of these tools, the helicon source, has been studied intensely by the UCLA group.

The problems of most concern no w are the interconnections between circuit layers and the damage to insulating layers that results from exposure to plasmas. By plasma induced damage one usually means the imbedding of charges inside the thin oxide layer that insulates the "gate" of a transistor, thus changing its electronic properties. Macroscopically, nonuniformities in plasma density, and hence of electric potential, can cause charges to build up across a wafer and be concentrated at one small point in a transistor. Microscopically, electric charges can build up on the sidewalls of a small trench being etched by plasma ions, thus altering their orbits and distorting the etched trench. These two problems are related when an imperfect trench allows charges to reach an otherwise protected oxide layer. Interconnections are made by etching very narrow, deep holes ("vias") from one layer to another and then filling the vias with a metal. This is now done without a plasma, so charging damage is not a problem; but in the future one may have to fill narrower deeper vias with ions from a metal plasma, and in that case one can anticipate charging problems.

Plasma-induced damage has become such an important topic that an international conference on it has been established. Some clever experiments have been done to elucidate and eliminate damage mechanisms, but these have almost all been in industrial laboratories in Japan. Aside from one outstanding group at Stanford, very little work of a fundamental nature has been done in the United States. This topic deserves more attention by plasma physicists in American universities.

II. INTRODUCTION

Plasma etching and deposition are essential for fabricating microelectronic circuits with sub-quarter-micron design rules, but unfortunately the electric charges in the plasma can damage the very elements that are being formed. This problem of device damage is currently the most pressing one in plasma processing. The delicate element that is of most concern is thin layer of insulating material, usually silicon dioxide, that separates the gate electrode from the conduction channel in a MOSFET. To reduce the overall size of transistors on a chip, these gate oxides are made as thin as 40-50 angstroms. When charges are buried in the oxide during plasma processing, the electrical characteristics of the transistor are changed, rendering it useless. The yield of good chips on a wafer depends critically on the probability of damage. Damage can be caused by ion bombardment, VUV radiation, exposure to hydrogen, or electron charges [12, 33]. This proposal addresses the most important of these: electron charging damage.

There are actually two effects of electron charging which require different methodologies for study. Macroscopic damage occurs when an imbalance in the plasma on a wafer size scale causes excess negative charge to collect on a network of conductors which focus the charge onto a gate oxide. The voltage across the oxide can be so large that it breaks down, but more likely, it just increases the small leakage current that always flows across the oxide (the Fowler-Nordheim or FN current), causing trapped holes to be formed inside the insulator.

Microscopic damage concerns the small trenches and holes that are etched or filled in the semiconductor material (Si). Straight sidewalls of these trenches or holes are produced when plasma ions are accelerated straight downwards by a plasma sheath, preparing the bottom of the trench for etching by Cl or F atoms via the well-known symbiotic process of reactive ion etching. If the sidewalls of the trench become charged, however, the ion orbits can be bent so that they hit the sidewalls, causing a phenomenon called "notching," a deformation of the bottom of the trench. This has been shown to arise from electron charges at the top of the trenches (called "electron shading," but it is not the same as oxide damage. The two phenomena are related, however, because this microscopic charging depends on the number of features in the surrounding area and so causes a nonuniformity in the rate of etching. During "overetch," an extended period needed to ensure that all the trenches have at least a minimum depth, some oxide layers may become exposed to plasma at their edges. These oxides can then be damaged not from the top, but from the side.

There is now an extensive literature on plasma-induced damage, and an international conference on this subject has been started; the first meeting was in Santa Clara in Feb. 1996. This wealth of information cannot be summarized in this short document, whose readers are probably more familiar with the subject than the author anyway. Most previous work has been of a statistical nature, showing the yield that is obtained under various processing conditions. The detailed mechanisms of charge-induced damage are still not fully understood. Several experiments of a fundamental nature, done in Japanese industrial laboratories, have been cleverly designed to clarify the physical mechanisms of damage. Except for McVittie's group at Stanford, we know of no other effort in the United States, in either universities or industry, that is doing as good a job as the Japanese in basic studies of charging damage mechanisms. Furthermore, there are few, if any, plasma physicists working on the problem. Since the motions of large numbers

of positive and negative charges are involved, plasma physicists are more likely to have the expertise to make significant progress toward understanding and eliminating charging damage.

The rationale for our proposal is based, therefore on the following points:

- Understanding charge damage requires enlisting the help of professional plasma physicists.
- Plasma physicists can help U.S. industry compete with Japan by working on this problem.
- Since future fabs will no doubt use HDP tools, the work is best done by a group that is familiar with HDPs and has the equipment to build and diagnose them.
- The UCLA group has a track record of being able to design and carry out experiments and calculations that elucidate the scientific basis behind complex phenomena.

Though we cannot foresee exactly what experimental and theoretical difficulties we will encounter, we would like to try.

III. MACROSCOPIC DAMAGE

Principal mechanisms. An n-channel MOSFET is schematically depicted in Fig. 1.

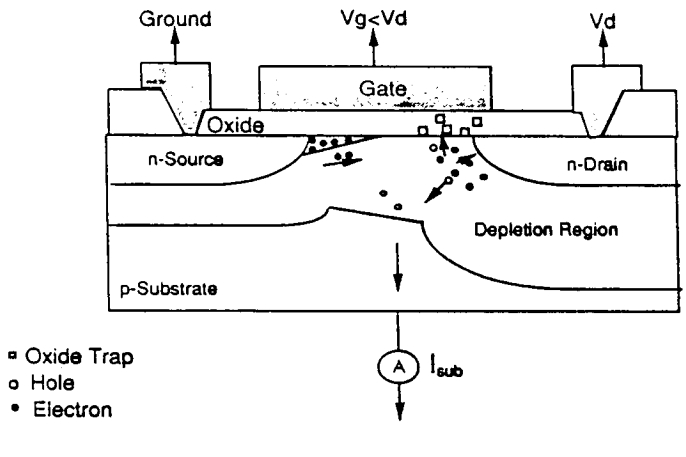

Fig. 1, Ref.[39]

It is part of a chip which might have features like those in Fig. 2 which have to be formed, layer by layer, by plasma processing. The gate

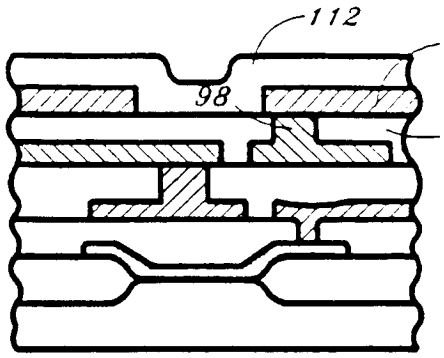

Fig. 2, Ref. [25]

voltage is isolated from the conduction channel by an oxide layer, which has to be thin compared with the size of the gate electrode. As all dimensions decrease, the oxide thicknesses are reduced below 50 A (Fig. 3). When electric charges collect on the oxide from either the top or the side (Fig. 4), charge

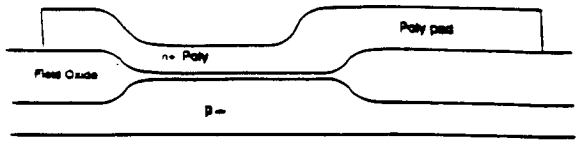

Fig. 3, Ref. [13]

traps and surface states can form, causing imperfections in the insulator. The damage is easily seen as a shift ΔV_{fb} in the flat-band voltage V_{fb}. In Fig. 5, it is seen that the energy levels in the Si, if they are flat, lie at least 3.1 eV below those in SiO_2. The capacitance between the gate and the substrate depends on the oxide thickness and the depth of the depletion layer formed when the gate is biased. This capacitance jumps between a high and a low level as the gate potential is varied past the threshold for forming a conduction channel, which is the voltage necessary to deplete the substrate carrier species (p, in Fig. 1) and attract the opposite species (n, in Fig. 1) so that the back-to-back diode configuration of the source and drain is eliminated. If charges are imbedded in the oxide, the threshold

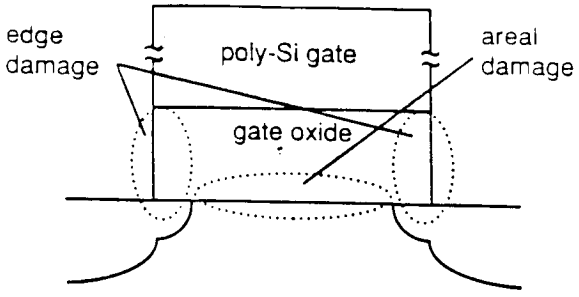

Fig. 4, Ref. [12]

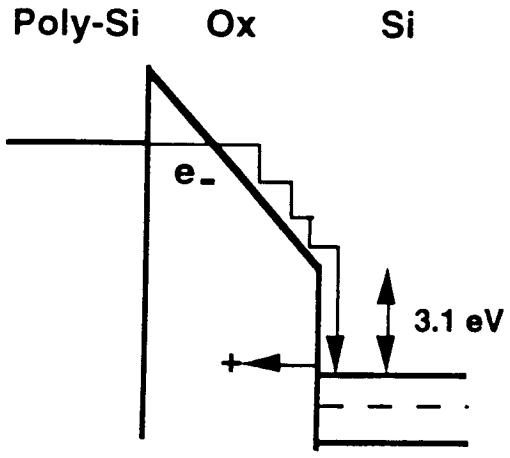

Fig. 5, Ref. [31]

voltage will change, as illustrated in Fig. 6 (for a *p*-MOS, since the threshold voltage is negative), changing the specifications of the transistor. These defects can be annealed by heating the device to, say, 200 C for half an hour, but the defects return under operation.

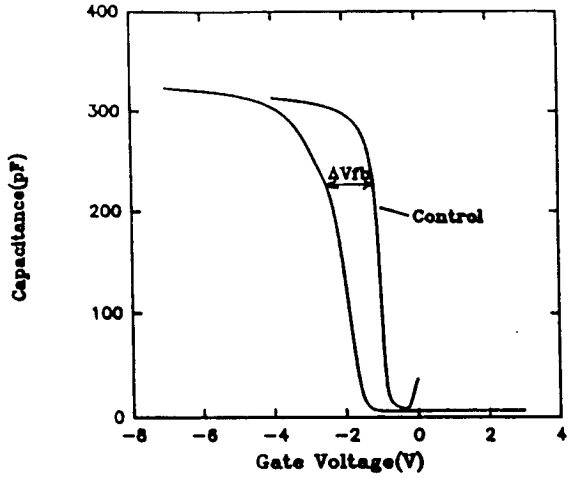

Fig. 6, Ref. [39]

During plasma processing, the substrate and the features on it are exposed to a plasma of density 10^{10}-10^{12} cm^{-3} through a sheath, which is generally much thicker than the feature sizes. Since electrons are much more mobile than ions, a sheath drop forms so that the plasma is just positive enough relative to the substrate that the Coulomb barrier makes the flux of electrons to the substrate

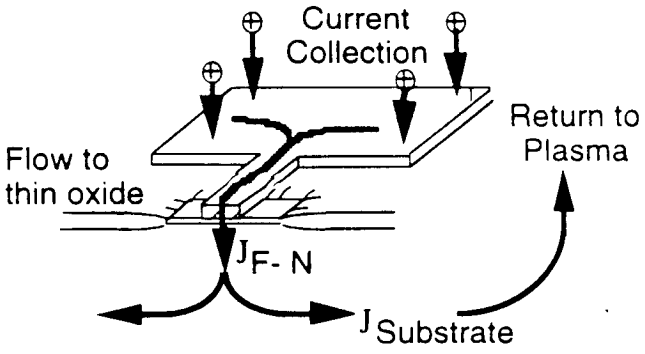

Fig. 7, Ref. [31]

equal to that of the ions. This is true over the entire wafer, since polysilicon is a poor conductor. However, there can be local imbalances so that a net positive or negative charge flows to the gate of a particular transistor, as shown in Fig. 7. In Fig. 8, the oxide layer is marked with the arrow labeled I_g. The sheath

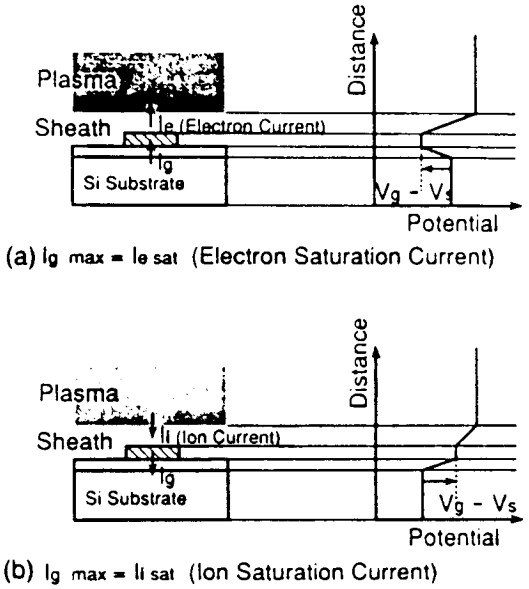

Fig. 8, Ref. [34]

drop is always negative, so that the gate electrode (shaded) is always negative relative to the plasma and communicates this potential to the top of the oxide. The bottom of the oxide is in contact with the Si substrate. Normally, an RF bias voltage is applied to the substrate so as to make the sheath drop larger by sheath rectification of the RF, in order to accelerate the ions to the design energy for etching. Although the impinging ions cannot respond to the RF frequency, the electrons can, and therefore the electron current to the gate fluctuates with the phase of the RF cycle, causing a net ion current to flow to the top of the oxide when the substrate is at its minimum voltage and a net electron current when the substrate is a its maximum voltage. If the oxide layer is thick, the top of it will charge up to the floating potential so that the ion and electron fluxes are always equal. If the oxide is thin, however, a tunneling current is driven through the oxide, as described below. Furthermore, the top and bottom of the oxide layer are electrically connected ac-wise by the large capacitance of the thin layer.

The magnitude of the E-field across the oxide can be very large, as seen in Fig. 9,

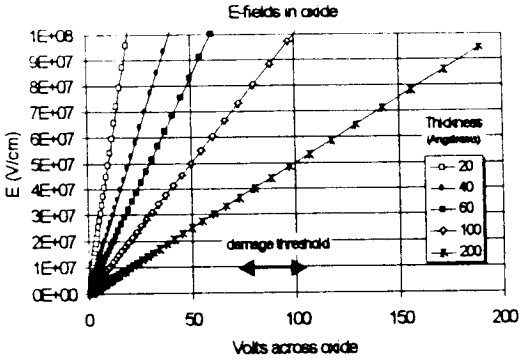

Fig. 9

where E is plotted against the voltage V across the insulator, where $V = V_{gate} - V_{substrate}$. For thin oxides and RF bias voltages of over 50 V, V can easily exceed the damage threshold of about 10^7 V/cm. In steady state, a small current tunnels through the potential barrier of Fig. 5 and allows a mismatch between the electron and ion currents impinging on the oxide. This leakage current, called the Fowler-Nordheim (FN) current, is shown in Fig. 10 vs.

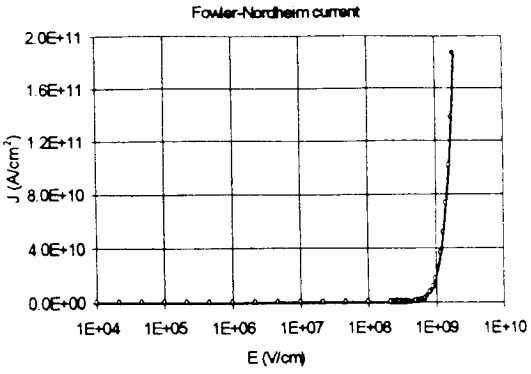

Fig. 10

E. It increases exponentially past an effective threshold of about 5×10^8 V/cm, according to the formula [39]

$$J_{FN} = AE^2 \exp(-B/E) \quad A/cm^2,$$
$$A = 1.54 \times 10^{-6} R/V_b \quad A/V^2, \tag{1}$$
$$B = 6.83 \times 10^7 V_b^{3/2}/\sqrt{R} \quad V/cm$$

where V_b is the barrier height, taken as 10 V in Fig. 10, and R is the ratio between the effective electron or hole mass in Si and in the insulator. Even before breakdown, however, the oxide is subject to a *Fowler-Nordheim stress current* equal to the difference between the ion and electron fluxes to the gate: $J_{FN} = e(J_i - J_e)$. These fluxes are given by probe theory:

$$J_e = n\left(\frac{KT_e}{2\pi m_e}\right)^{1/2} \exp(-V_s/KT_e),$$
$$J_i = 0.5n\left(\frac{KT_e}{M_i}\right)^{1/2} \tag{2}$$

where n is the plasma density and V_s the potential of the plasma relative to the gate. The current that flows through a thin oxide is at the intersection of the $J_i - J_e$ curve and the J_{FN} curve, as shown in Fig. 11 for two oxide

thicknesses. This steady-state current builds up a charge Q on the surface of the oxide of just

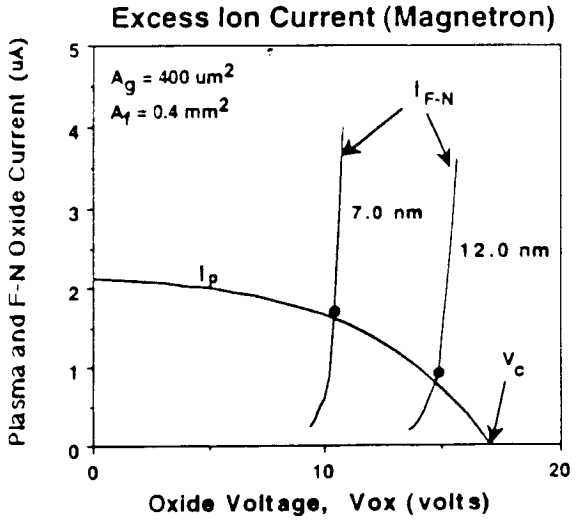

Fig. 11, Ref. [31]

the right magnitude to give the required FN current, according to Figs. 9 and 10. The charge Q is given by the capacitance C of the oxide layer times the voltage V across it.

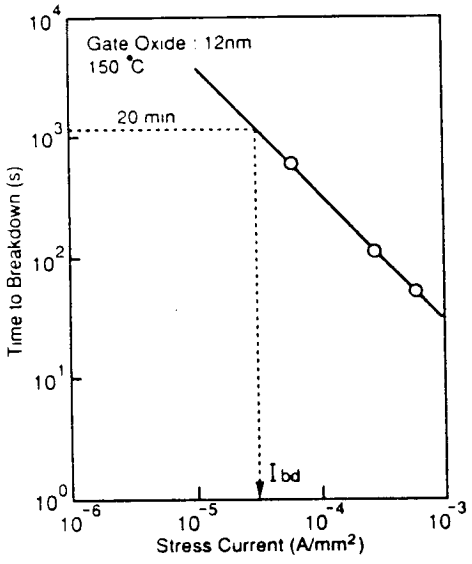

Fig. 12, Ref. [34]

When Q exceeds a critical value Q_{bd}, breakdown occurs. The reason that Q_{bd} is usually quoted rather than V_{bd} is that C is proportional to $1/d$, where d is the oxide thickness, while $E \propto V/d$; hence, $Q = CV \propto d^{-1}Ed \propto E$, independently of d (*cf.* Fig. 10). In experiments where a controlled FN stress current is applied [1], breakdown occurs after the time necessary to build up Q_{bd}, as shown in Fig.12.

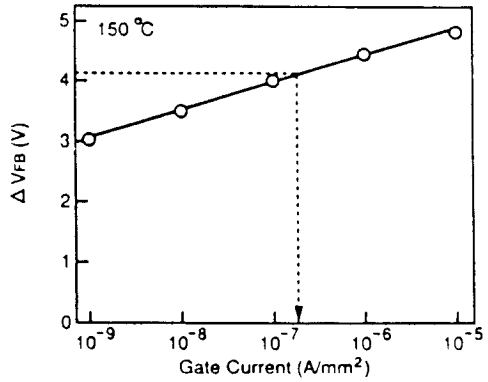

Fig. 13, Ref. [34]

At currents smaller than this, damage is still occurring, as evidenced by the increase in ΔV_{fb}, as shown in Fig. 13.

State of knowledge. The antenna effect has been well documented. For a given current imbalance J_i - J_e, the amount of charge impinging on a gate depends on the area of conductors connected to the gate (Figs. 2 and 7). The antenna ratio, defined in Fig. 14, can exceed 10^4. The increased damage caused by large antenna ratios is illustrated in Figs. 14

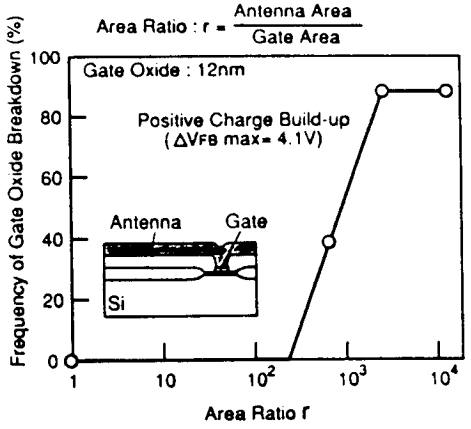

Fig. 14, Ref. [34]

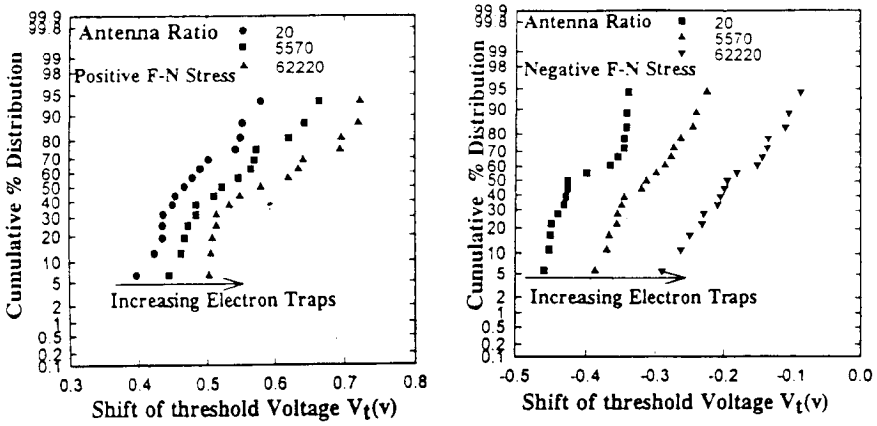

Fig. 15, Ref. [39]

and 15. Note also in Fig. 14 that the damage is larger for negative FN stress for reasons that are not clear [1], but perhaps because the potential barrier of Fig. 5 is obviously lower in that case. This dependence on the sign of the gate voltage is also shown in Fig. 16, and the

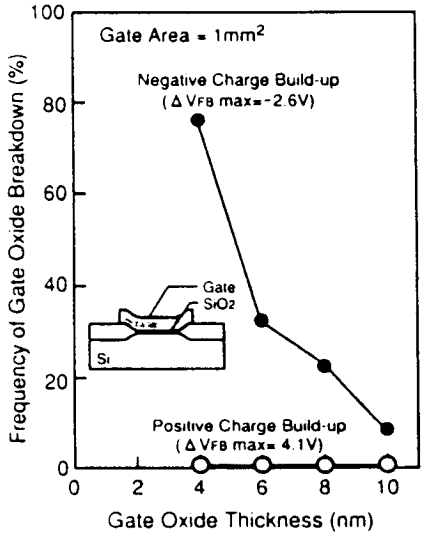

Fig. 16, Ref. [33]

asymmetry between *p*-MOS and *n*-MOS has been documented by Li et al. [27].

Plasma inhomogeneity has been shown to cause the current inequalities that can cause charges to collect on an antenna. The idea is shown in Fig. 17. If the plasma density is nonuniform, the Boltzmann relation $n_e = n_o \exp(eV_s/KT_e)$ will cause the plasma potential to be nonuniform also. There may also be gradients in KT_e, but electron heat conduction is usually so large that these would be very small. From Eq. (2) we see that J_e cannot be equal to J_i everywhere if V_s varies, so an FN stress is imposed at least in some regions of the wafer. Fig. 18 is a reminder that V_s can vary with the RF cycle if either the substrate fluctuates due to a bias oscillator or the plasma fluctuates due to the ionizing field.

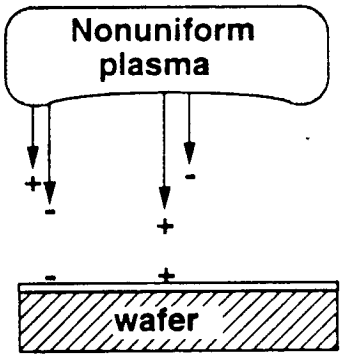

Fig. 17, Ref. [32]

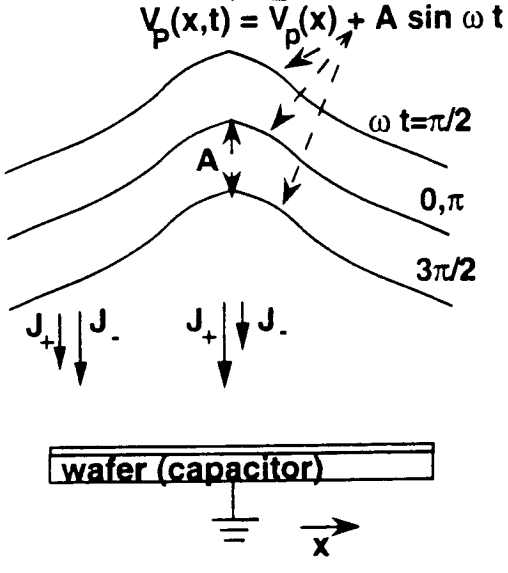

Fig. 18, Ref. [32]

Magnetic fields parallel to the wafer can increase damage by disrupting the motion of electrons and making J_e - J_i larger. Several

papers in recent years have addressed the problem of the magnetic sheath that forms when the field lines are at an angle to the surface. Fig. 19 shows the type of experiments

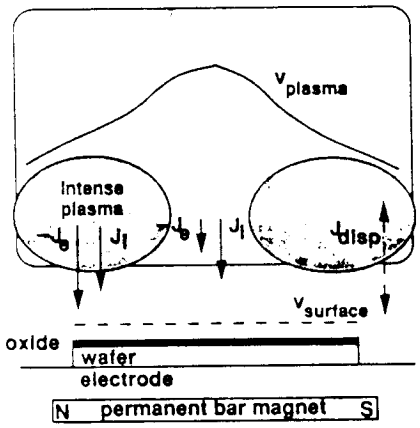

Fig. 19, Ref. [10]

that have been done by introducing an arbitrary, nonuniform magnetic field. Fig. 20 shows that, in a capacitive RIE discharge, both V_{fb} and the gate breakdown voltage worsen with a magnetic field at the wafer position.

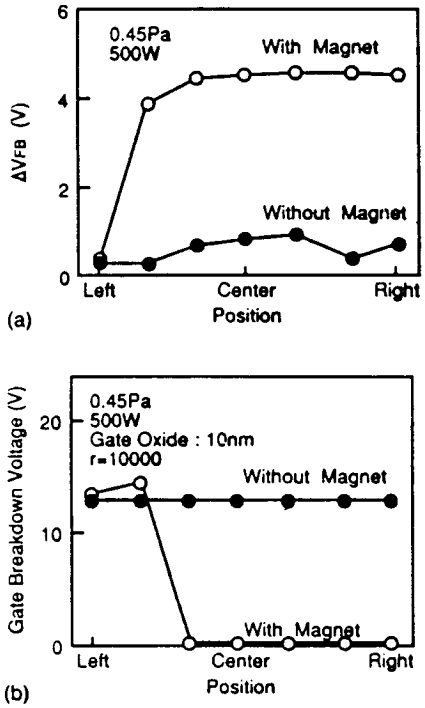

Fig. 20, Ref. [34]

Electron temperature can affect damage because, according to Eq. (2), any change in J_e due to a change in V_s would scale with KT_e. This is shown in Fig. 21, in which the variation of KT_e over the wafer was measured,

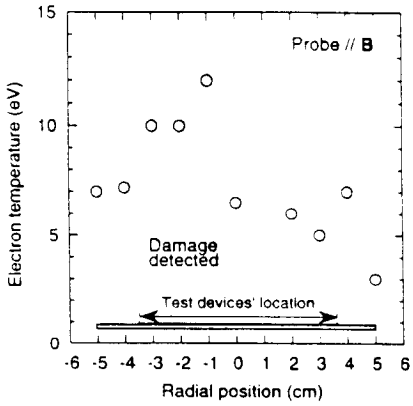

Fig. 21, Ref. [19]

and damage was detected only in the region where KT_e was high. The decay of the plasma after the end of a pulse has been measured and modeled by Ashida et al. [2]. Hashimoto *et al.* [19] have done a neat experiment demonstrating how to minimize damage by lowering the electron temperature. By pulsing the plasma

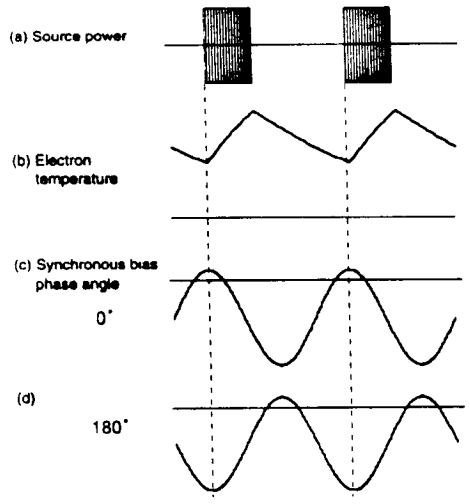

Fig. 22, Ref. [19]

source, they could see KT_e decaying in the afterglow (Fig. 22). By phasing the bias oscillator relative to the plasma source pulses, they could control the ion energy and therefore make the etching occur when KT_e was either

high or low. Fig. 23 shows the damaged devices on a test wafer, with much less damage correlating with low electron temperature.

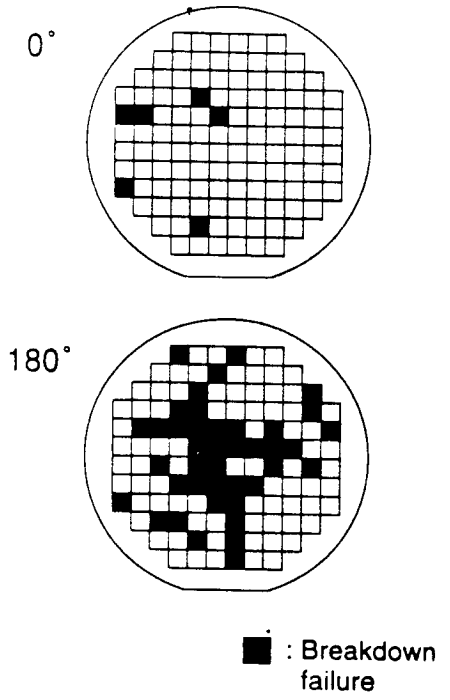

Fig. 23, Ref. [19]

Dependence on the etch cycle has been shown. Fig. 24 shows how, even when the antenna is covered with oxide, current can go sideways into the antenna when the oxide is

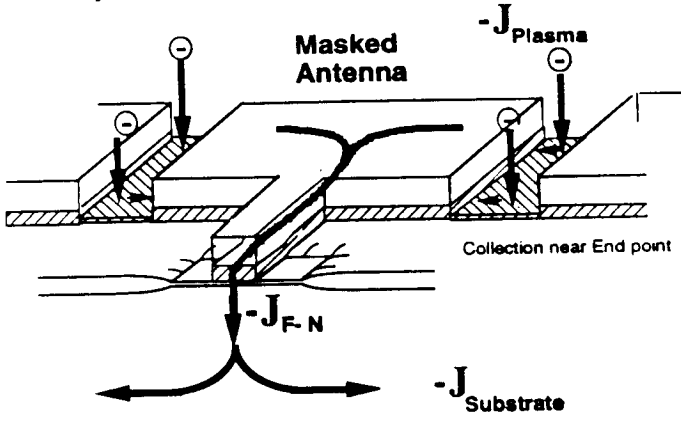

Fig. 24, Ref. [31]

etched through. Fig. 25 shows the shift ΔV_{fb} induced by an overetch. The damage as a function of overetch percentage has been measured by Gabriel and McVittie [16]. Fig. 26 shows a case where damage occurs not

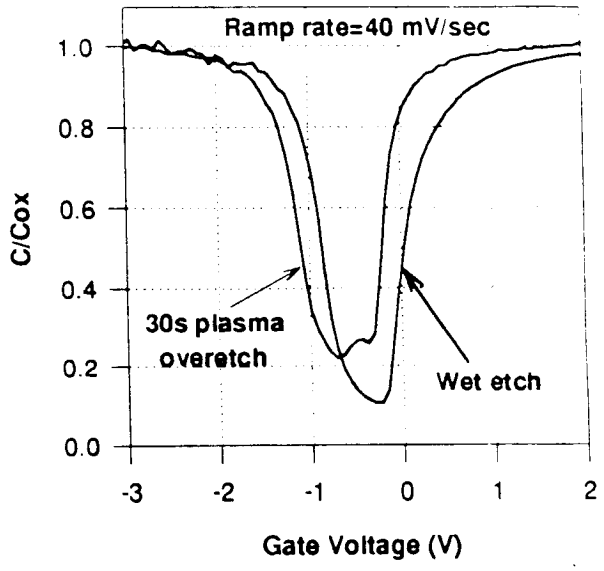

Fig. 25, Ref. [38]

during an overetch but just before it.

When the polysilicon layer is thick, excess charges can be conducted away to other parts of the circuit. When the polysilicon layer is completely removed, directed ion currents fall only on the (thick) field oxide, where they induce innocuous charges. However, when the polysilicon layer has been reduced to a thin layer but is still there, it can collect ion charges but cannot conduct them far away because of its small (500 Ω-cm) conductivity; the charges must then flow through the thin oxide as a FN current.

Measuring damage has become such a big problem that two types of diagnostic wafers have been developed. The SPORT wafer [36] (Figs. 27, 28) makes real-time measurements of the charge impinging at different points on a wafer by a series of aluminum pads connected to coaxial cables. The CHARM-2 wafer is covered with EEPROM devices (Fig. 29) which can record the time-integrated potential or charge at each point on the wafer. These are read afterwards to give a display like that in Fig. 30. SPIDER (SEMATECH Process Induced Damage Effect Revealer) test structures are

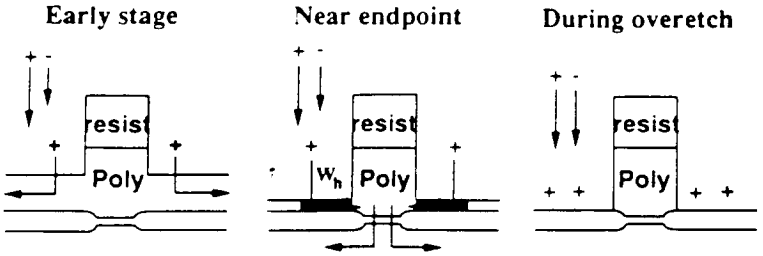

Fig. 26, Ref. [32]

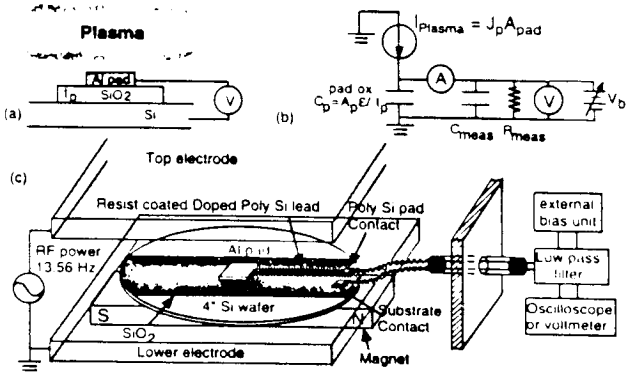

Fig. 27, Ref. [28]

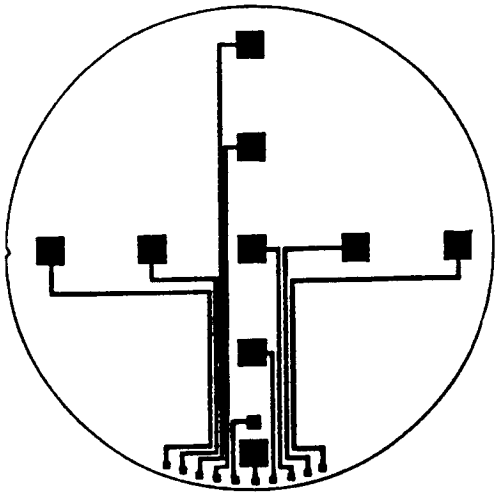

Fig. 28, Ref. [36]

transistors with gates connected to different antennas and thus can test damage of actual devices [3, 28].

Much of the work so far has been of a practical nature, measuring the probability of damage under various processing conditions without regard for the physical mechanisms involved. The early work was done in capacitive RIE (reactive ion etching) [40] or magnetron [10] discharges, where the large oscillations in plasma potential made interpretation difficult. There have been more recent experiments done on ECR (electron cyclotron resonance) discharges [33]. More recently, Blayo et al. [5] compared the damage observed with ECR and helicon discharges. Chemical downstream etching was compared with plasma etching and was found to be not free of charge damage effects [6, 4]. Damage occurs not only in etching but also in deposition [7], especially in HDP sources [23]. Oxide damage can also occur from hot-carrier injection, and this has been compared with dielectric breakdown by Li et al. [26]. Yonugami et al. have done an interesting experiment with injection of low-energy electrons showing that damage can be caused by phonon excitation [41].

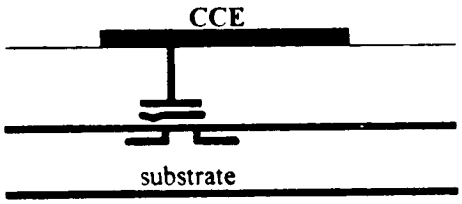

Fig. 29, Ref. [28]

Modeling of many observed effects has been done successfully by McVittie and his coworkers [9-11, 14-16, 20-22, 29-32, 36]. The most complete modeling effort so far, by En et al. [8] incorporates not only the equivalent circuits of IC devices but also the plasma and sheath effects, including plasma inhomogeneity.

IV. MICROSCOPIC DAMAGE

The electron shading effect is illustrated in Fig. 31. Here the diagonal shading indicates the Si layer being etched; above it is the photoresist, and below it the oxide insulator. Electrons are isotropic and therefore strike the photoresist from all sides, charging it negative. This charge is not shielded because

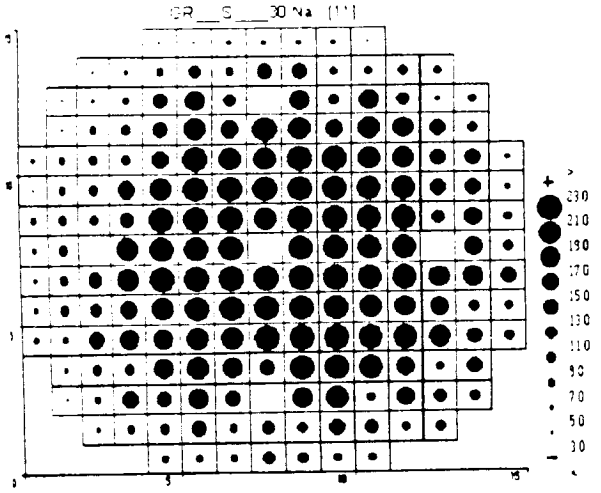

Fig. 30, Ref. [28]

the Debye length is large on this scale, and it repels electrons, causing their flux to the bottom of the trench to be greatly diminished.

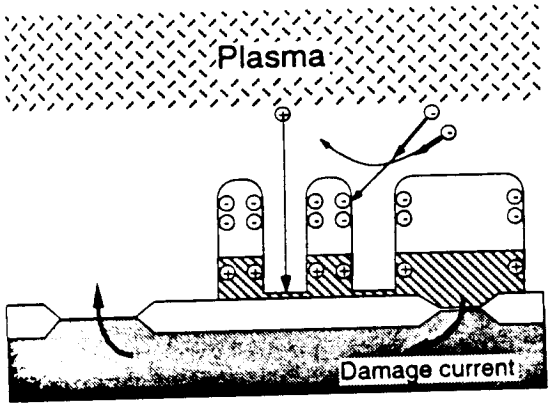

Fig. 31, Ref. [19]

The ions, however, are accelerated straight downwards by the sheath potential and are supposed to reach the bottom of the trench, preparing the area for efficient etching by neutral Cl atoms. However, the electron charges on the top of the trench, if they are not symmetric, can distort the ion orbits so that the ions strike the sidewalls at the bottom, charging them positive. A self-consistent distribution of potentials and ion orbits is then formed. If the features are not all the same size, the charging of the sidewalls will not be symmetric. In particular, the outside wall of the end line is not shielded from the electrons, and should not have a large positive charge at the bottom. The charge distribution inside a trench has been modeled, usually by Monte-Carlo calculations with Maxwellian electrons and self-consistent ion orbits. An example is shown in Fig. 32. The bending of the ion orbits causes "notching" at the bottom of the etched trenches (except the one at the end line) [20, 21]. A thorough modeling of this effect has been done by Kinoshita et al. [22]. This notching effect even occurs with neutral beam etching, and this has been observed and modeled in detail by Giapis (private communication, submitted to JVSTB). Guard electrodes have been used to minimize the endline effect [35]. The literature on trench deformations is very large and will not be summarized here.

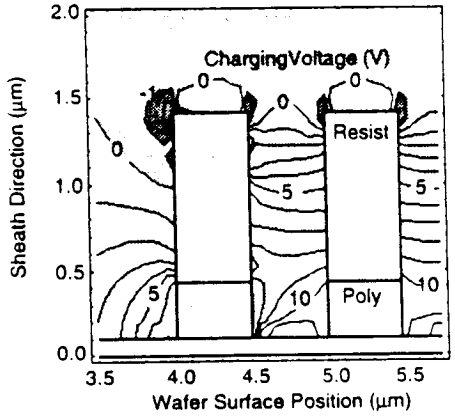

Fig. 32, Ref. [22]

The connection between electron shading and oxide damage can be seen in Fig.

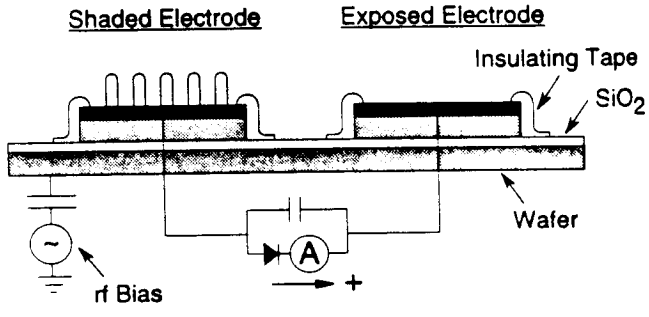

Fig. 33, Ref. [19]

31. The positive charges that collect at the bottom of the trenches appears at the gate electrode, where they induce a Fowler-Nordheim current to close the current loop. This current has been measured directly by Hashimoto et al. [19] with the apparatus shown in Fig. 33. The Si layer with structures on it gets a net positive charge compared with an unshaded layer that is receives equal numbers of ions and electrons. By pulsing the discharge and changing the phase of the bias voltage relative to the plasma pulses, as described earlier, it is seen in Fig. 34 that the differential current measured by the ammeter in Fig. 33 is larger with the phase corresponding to higher KT_e and higher damage.

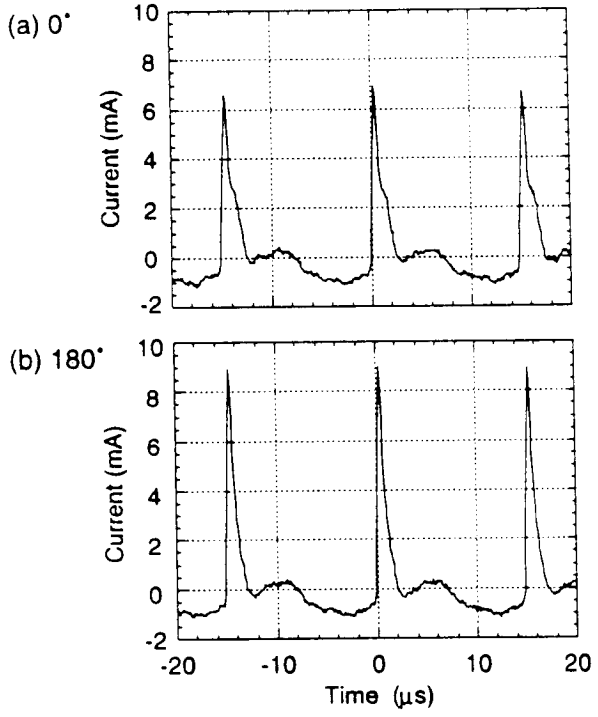

Fig. 34, Ref. [19]

The advent of HDP tools has permitted careful documentation of the notching effect. However, very few basic experiments designed to verify the details of the process have been done so far. Besides the Hashimoto [19] experiment described above, the most clever one that we have seen so far is that of Kurihara and

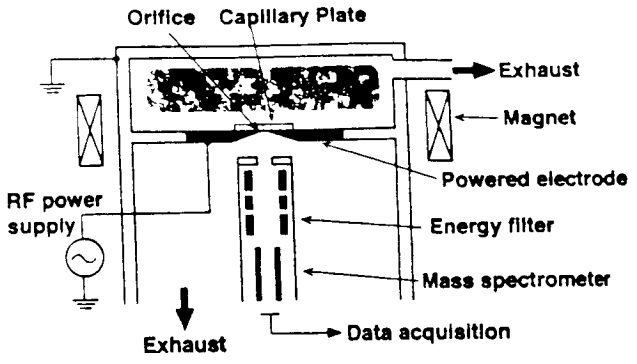

Fig. 35, Ref. [24]

Sekine [24], whose apparatus is shown in Fig. 35. The wafer on the powered electrode of an RIE discharge was drilled with a 200-μm hole. Over this was placed a lead-glass capillary plate with 10-μm holes of different aspect ratios (lengths). Analysis of ions of different species accelerated in the sheath and passing through the holes was made by a quadrupole mass analyzer. Fig. 36 shows the ion energy distribution for various aspect ratios AR. For

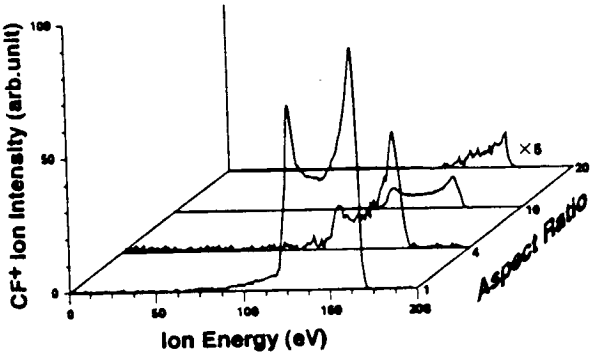

Fig. 36, Ref. [24]

AR = 1, the double-peaked time-averaged distribution typical of RIE discharges is seen. The low- and high-energy peaks are caused by the long time spent by the powered electrode at the maximum and minimum potential periods of the RF cycle. For high AR, it is seen that the low energy ions do not make it through the hole. Presumably, ions hitting the sidewalls charge them up, thus creating a potential peak and preventing low-energy ions from getting through. To show this, Kurihara

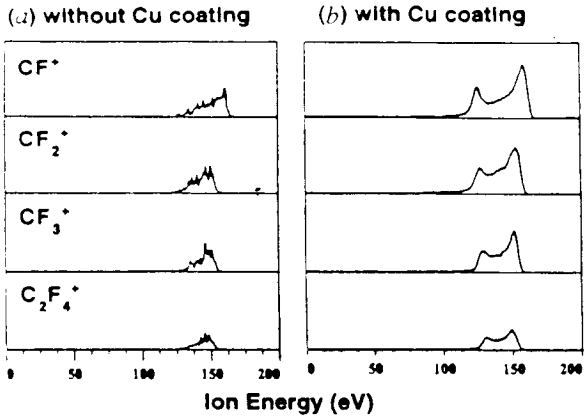

Fig. 37, Ref. [24]

et al. coated the sidewalls with conductive Cu, thus preventing the charge accumulation. Fig. 37 shows that the low-energy peak returns in this case. This is an example of the type of basic experiments needed in this field.

V. TOPICS FOR FURTHER STUDY

- Relation of charging currents to well-documented plasma conditions
- Measurements of potentials and currents on substrates using RF-compensated electrodes
- Effect of uniform magnetic fields to charging currents, together with theory
- Time-resolved measurements correlating damage with the RF cycle
- Separation of RF effects due to source and to bias oscillator
- Tailoring of high-density RF sources to produce low T_e , ion energies, B-fields, and density gradients at wafer
- Control of density and potential gradients in large-area sources to reduce damage
- Effects of fields arising from electrostatic chucks
- Effects of pulsed plasmas
- Effects of negative ions
- Dependence of electron shading effect on geometry and local conductivities
- Possible charging effects in the deposition of metals into high aspect rato vias

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